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Low Temperature Deposition and Characterization of N- and P-Type Silicon Carbide Thin Films and Associated Ohmic and Schottky Contacts

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13. ABSTRACT ***(Maximum 200 words)***

Exposure of heated 6H-SiC wafers to SiH_4 contained both in a gas stream and an activated plasma was investigated for low temperature SiC cleaning and oxygen removal prior to thin film deposition. UPS revealed the first observation of surface states on the cleaned 6H-SiC surface. Monocrystalline epitaxial films of β(3C)-SiC(111) and α(6H)-SiC(0001) were grown on vicinal (~3.5° off (0001) towards) α(6H)-SiC(0001) substrates via gas-source MBE from 1050 to 1250°C using Si_2H_6 and C_2H_4. Undoped films were n-type; p-type films were achieved using Al evaporation during growth. The undoped 3C-SiC films grown on thin AlN buffer layers had carrier concentrations as low as 3×10^{15} cm^{-3}. Extremely efficient activation of p-type (Al) dopants has been achieved. Initial attempts at n-type doping using NH_3 are also described. Surfaces of 6H-SiC(0001) homoepitaxial layers deposited on vicinal and on-axis 6H-SiC wafers by CVD have also been investigated using ultra-high vacuum scanning tunneling microscopy (UHV STM). The vicinal surface showed strongly undulating step configurations. The on-axis surface possessed much wider terraces and much smoother step undulations. Step heights on both surfaces were ~2.5 Å corresponding to a single bilayer containing one Si and one C layer. After annealing at T>1100 °C for 3-5 min. in UHV, selected terraces contained honeycomb-like regions most likely caused by the transformation to graphite as a result of Si sublimation. Thin films (4 - 1000Å) of Pt contacts were also deposited via UHV electron beam evaporation at room temperature on n-type α(6H)-SiC (0001) substrates and examined in terms of chemistry, microstructure, and electrical properties. The as-deposited contacts were polycrystalline and showed excellent rectifying behavior with low ideality factors ($n < 1.1$) and leakage currents of 5×10^{-8} A/cm² at -10 V. The Schottky barrier height increased from 1.06 eV before annealing to 1.26 eV after successive 20 min. anneals at 450, 550, 650, and 750°C. The leakage current decreased to 2×10^{-8} A/cm² at -10 V. Interfacial reactions were not observed at T<750°C; above this temperature, Pt_2Si and C precipitates were identified in the reaction zone.

14. SUBJECT TERMS

epitaxial films, β-SiC, 6H-SiC, MBE, n-type, p-type, AlN buffer layer, cleaning, SiH_4, oxygen removal, scanning tunneling microscopy, STM, vicinal surface, graphite, Schottky contacts, Pt, Schottky barrier, leakage current, Pt_2Si, C, precipitates

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I. Introduction

Silicon carbide (SiC) is a wide bandgap material that exhibits polytypism, a one-dimensional polymorphism arising from the various possible stacking sequences of the silicon and carbon layers. The lone cubic polytype, β-SiC, crystallizes in the zincblende structure and is commonly referred to as 3C-SiC. In addition, there are also approximately 250 other rhombohedral and hexagonal polytypes [1] that are all classed under the heading of α-SiC. The most common of the α-SiC polytypes is 6H-SiC, where the 6 refers to the number of Si/C bilayers along the closest packed direction in the unit cell and the H indicates that the crystal structure is hexagonal.

Beta (3C)-SiC is of considerable interest for electronic applications that utilize its attractive physical and electronic properties such as wide bandgap (2.2 eV at 300K) [2], high breakdown electric field (2.5×10^6 V/cm) [3], high thermal conductivity (3.9 W/cm °C) [4], high melting point (3103K at 30 atm) [5], high saturated drift velocity (2×10^7 m/s) [6], and small dielectric constant (9.7) [7]. Primarily due to its higher electron mobility than that of the hexagonal polytypes, such as 6H-SiC [8], β-SiC remains preferable to hexagonal SiC for most device applications.

Most 3C-SiC thin film growth to date has been performed on Si substrates. Large-area, crack-free, and relatively thick (up to 30 μm) epitaxial 3C-SiC thin films have been grown on Si (100) by exposing the Si substrate to a C-bearing gaseous species prior to further SiC growth [7, 9, 10]. However, these films exhibited large numbers of line and planar defects due to large lattice and thermal mismatches between SiC and Si. One particular type of planar defect, the inversion domain boundary (IDB), was eliminated with the use of Si (100) substrates cut 2°–4° toward [011] [11–13]. Growth on Si substrates has allowed much understanding of SiC growth processes and device development to occur, but the large thermal and lattice mismatches between SiC and Si hamper further development using Si substrates. As a result, great effort has been made to develop methods for growth SiC single crystal substrates for homoepitaxial growth of SiC thin films.

Since the 1950's, monocrystalline single crystals of 6H-SiC have been grown at using the Lely sublimation process [14]. However, nucleation was uncontrolled using this process and control of resultant polytypes was difficult. SiC single crystals inadvertently formed during the industrial Acheson process have also been used as substrates for SiC growth. However, neither these crystals or those formed using the Lely process are large enough for practical device applications. Recently, using a seeded sublimation-growth process, boules of single polytype 6H-SiC of > 1 inch diameter of much higher quality of that obtained using the Lely process have been grown. The use of single crystals of the 6H polytype cut from these boules has given a significant boost to SiC device development.

Silicon carbide epitaxial thin film growth on hexagonal SiC substrates has been reported since the 1960's. The use of nominally on-axis SiC substrates has usually resulted in growth of 3C-SiC films. Films of 3C-SiC (111) grown by CVD have been formed on 6H-SiC substrates less than 1° off (0001) [15]. Films of 3C-SiC on 6H-SiC substrates have typically had much lower defect densities than those grown on Si substrates. The major defects present in 3C-SiC/6H-SiC films have been double positioning boundaries (DPB) [16]. Despite the presence of DPBs, the resultant material was of sufficient quality to further device development of SiC. The use of off-axis 6H-SiC (0001) substrates has resulted in growth of high-quality monocrystalline 6H-SiC layers with very low defect densities [17].

In addition, the use of more advanced deposition techniques, such as molecular beam epitaxy (MBE), has been reported for SiC in order to reduce the growth temperature and from about 1400–1500°C on 6H-SiC substrates. Si and C electron-beam sources have been used to epitaxially deposit SiC on 6H-SiC (0001) at temperatures of 1150°C [18]. Ion-beam deposition of epitaxial 3C-SiC on 6H-SiC has also been obtained at the temperature of 750°C using mass-separated ion beams of $^{30}Si^{+}$ and $^{13}C^{+}$ [19].

Aluminum nitride (AlN) is also of particular interest at this time because of its very large bandgap. It is the only intermediate phase in the Al-N system and normally forms in the wurtzite (2H-AlN) structure. Most current uses of AlN center on its mechanical properties, such as high hardness (9 on Mohs scale), chemical stability, and decomposition temperature of about 2000°C [20]. Properties such as high electrical resistivity (typically $\geq 10^{13}$ Ω-cm), high thermal conductivity (3.2 W/cm K) [21], and low dielectric constant ($\varepsilon \approx 9.0$) make it useful as a potential substrate material for semiconductor devices as well as for heat sinks. The wurtzite form has a bandgap of 6.28 eV [22] and is a direct transition, thus it is of great interest for optoelectronic applications in the ultraviolet region.

Because of the difference in bandgaps (2.28 eV for 3C-SiC and 6.28 eV for 2H-AlN) between the materials, a considerable range of wide bandgap materials, made with these materials, should be possible. Two procedures for bandgap engineering are solid solutions and multilayers. A particularly important factor is that the two materials have a lattice mismatch of less than one percent.

Research in ceramic systems suggests that complete solid solubility of AlN in SiC may exist [23]. Solid solutions of the wurtzite crystal structure should have E_g from 3.33 eV to 6.28 eV at 0 K. Although it has not been measured, the bandgap of cubic AlN has been estimated to be around 5.11 eV at absolute zero and is believed to be indirect [24]. Cubic solid solutions should thus have E_g from 2.28 eV to roughly 5.11 eV at 0 K and would be indirect at all compositions if theory holds true.

Because of their similarity in structure and close lattice and thermal match, AlN-SiC heterostructures are feasible for electronic and optoelectronic devices in the blue and infrared

region. Monocrystalline AlN layers have been formed by CVD on SiC substrates [25] and SiC layers have been formed on AlN substrates formed by AlN sputtering on single crystal W [26]. In addition, theory on electronic structure and bonding at SiC/AlN interfaces [24] exists and critical layer thicknesses for misfit dislocation formation have been calculated for cubic AlN/SiC [27]. Note that AlN (at least in the wurtzite structure) is a direct-gap material and SiC is an indirect gap material. Superlattices of these materials would have a different band structure than either constituent element. The Brillouin zone of a superlattice in the direction normal to the interfaces is reduced in size. This reduction in zone size relative to bulk semiconductors causes the superlattice bands to be "folded into" this new, smaller zone. This folding can cause certain superlattice states to occur at different points in k space than the corresponding bulk material states [28]. This can lead to direct transitions between materials which in the bulk form have indirect transitions. This has been demonstrated in the case of $GaAs_{0.4}P_{0.6}$/GaP and $GaAs_{0.2}P_{0.8}$/GaP superlattices, where both constituents are indirect in the bulk form [29]. Whether this is possible in the case of AlN/SiC is unknown, but very intriguing. It may be possible to obtain direct transitions throughout nearly the entire bandgap range with use of superlattices of AlN and SiC. Use of solid solutions in superlattices introduces additional degrees of freedom. For example, the bandgap can be varied independently of the lattice constant with proper choice of layer thickness and composition if superlattices of solid solutions of AlN and SiC were formed.

Due to the potential applications of solid solutions and superlattice structures of these two materials, an MBE/ALE system was commissioned, designed, and constructed for growth of the individual compounds of SiC and AlN, as well as solid solutions and heterostructures of these two materials. Dithisimal studies concerned with the kinetics and mechanisms of mass transport of Si, C, Al and N at the SiC/AlN interface are also being conducted in tandem with the deposition investigations.

A very important additional goal of this research is to understand what controls the contact electrical characteristics of specific metals to n-type 6H-SiC and to use this information to form good ohmic and Schottky contacts. A list of five metals to be studied, which consists of Ti, Pt, Hf, Co, and Sr, was created at the beginning of this research project. The selection process began by taking the simplest case, an ideal contact which behaves according to Schottky-Mott theory. This theory proposes that when an intimate metal-semiconductor contact is made the Fermi levels align, creating an energy barrier equal to the difference between the workfunction of the metal and the electron affinity of the semiconductor. It is the height of this barrier which determines how the contact will behave; for ohmic contacts it is desirable to have either no barrier or a negative barrier to electron flow, while for a good Schottky contact a large barrier is desired.

Although metals were chosen optimistically, i.e. on the basis that they will form ideal contacts, some evidence exists that the contact properties will be more complicated. J. Pelletier *et al.* [30] have reported Fermi level pinning in 6H-SiC due to intrinsic surface states, suggesting little dependence of barrier height on the workfunction of the metal. In addition, L. J. Brillson [31, 32] predicts the pinning rate to be higher for more covalently bonded materials. Other complications may arise if the surface is not chemically pristine. A major part of this project will be devoted to determining whether the contacts behave at all ideally, and if not, whether the Fermi level is pinned by intrinsic or extrinsic effects.

Along with examining the barriers of the pure metal contacts, the chemistry upon annealing will be studied and correlated with the resulting electrical behavior. The electrical behavior will be quantified both macroscopically in terms of current-voltage characteristics and microscopically in terms of barrier height. Identification of the phases formed will present the opportunity to attribute the electrical characteristics to the new phase in contact with silicon carbide.

Within this reporting period, investigations concerned with (1) growth of monocrystalline epitaxial films of β(3C)-SiC(111) and α(6H)-SiC(0001) on vicinal (~3.5° off (0001) towards <11$\bar{2}$0>) α(6H)-SiC(0001) substrates via gas-source MBE, (2) n- and p-type doping of these films with N and Al, respectively, (3) cleaning and oxygen removal via exposure to SiH_4 in a gas stream and in a plasma, (4) STM of homoepitaxial 6H-SiC film surfaces and (4) the deposition, annealing and electrical and microstructural characterization of Pt Schottky contacts have been conducted. Extremely efficient activation of p-type (Al) dopants has been achieved. UPS revealed the first observation of surface states on the clean 6H SiC surface after cleaning with SiH_4. The vicinal surface examined via STM showed strongly undulating step configurations. The on-axis surface possessed much wider terraces and much smoother step undulations. Step heights on both surfaces were ~2.5 Å corresponding to a single bilayer containing one Si and one C layer. The as-deposited Pt Schottky contacts were polycrystalline and showed excellent rectifying behavior with low ideality factors ($n < 1.1$) and leakage currents of 5×10^{-8} A/cm^2 at -10 V. The Schottky barrier height increased from 1.06 eV before annealing to 1.26 eV after successive 20 min. anneals at 450, 550, 650, and 750°C. The leakage current decreased to 2×10^{-8} A/cm^2 at -10 V. Interfacial reactions were not observed at T<750°C; above this temperature, Pt_2Si and C precipitates were identified in the reaction zone.

The experimental procedures, results, discussion of these results, conclusions and plans for future efforts for each of the topics noted above are presented in the following sections. Each of these sections is self-contained with its own figures, tables and references.

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II. Silane Plasma and CVD Preparation of 6H SiC Surfaces for Growth of Epitaxial Films

A. Introduction

As the need increases for electronic devices that have higher performance characteristics, surface cleaning without damage becomes especially important. Hydrogen plasma processing have been demonstrated in cleaning silicon wafers.[1] Recently, silane/hydrogen mixtures have been used to clean silicon.[2] As SiC tends to graphitize with annealing, this technique should work for SiC. R. Kaplan has investigated this by annealing ß and 6H SiC samples in a silicon flux.[3] We demonstrate in this report surface cleaning of 6H SiC both by silane (SiH_4) chemical vapor deposition (CVD) and by silane plasma treatment.

UPS is used to examine the electronic states of the processed surface. Surface states, possibly caused by dangling bonds on a clean surface, are observed. Surface states appear as distinctive features in the spectra.

B. Experimental Procedures

These studies have been performed in an integrated vacuum transfer system. The capabilities include plasma processing, UPS, XPS, MBE, LEED and Auger electron spectroscopy (AES).

The plasma system has a base pressure of 1.0×10^{-9} Torr but operates in the milliTorr range of pressure. Hydrogen of up to 100 sccm can flow into the system. One may also flow at a rate of 10 sccm, a mixture of 1% silane/H_2. Power is coupled into the chamber through rf induction. Typical values are from 20 to 400 watts depending on the type of cleaning/etching desired. Figure 1 depicts the chamber.

We have cleaned the surface two different ways. Both involve an *ex situ* HF dip to remove thick oxide. The first method is simply to anneal the sample in a silane flux. A temperature of 825 °C is reached and held for 5 minutes in a flow of 10 sccm of 1% silane/H_2. AES of this process, along with the LEED pattern, is shown in Fig. 2 and compared to an *ex situ* clean. The second method involves the rf plasma. The effect of this processing is shown in Fig. 3. Our parameters are: a temperature of 800 °C, power of 400 watts, a flow of 10 sccm, and a pressure of 25 mTorr. Both parameters result in substantial removal of oxygen and surface hydrocarbons. The CVD clean results in a 3×3 reconstruction, possibly due to a silicon adatom structure, indicating a Si rich surface.[4] The plasma clean results in a 1×1 surface showing the stoichiometry of the bulk.

The UPS chamber has a base pressure of 2×10^{-10} Torr. Operating conditions involve pressures up to 1×10^{-9} Torr, but the higher pressure is due to the helium inflow and does not contaminate the sample. The UPS system utilizes a helium resonance lamp (the He I line) to

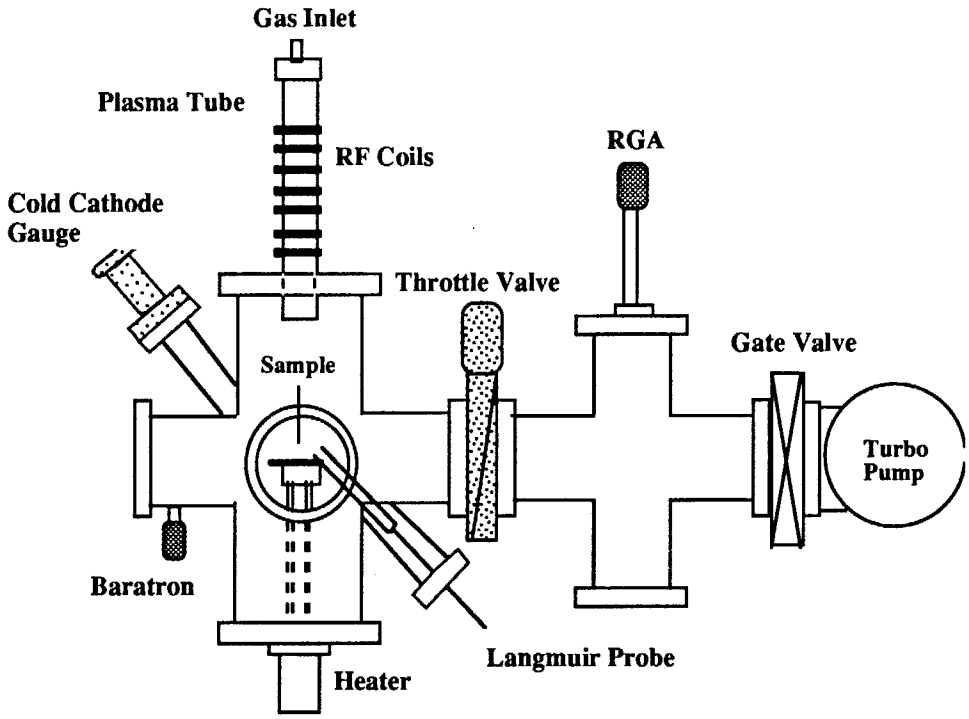

Figure 1. The plasma/CVD chamber.

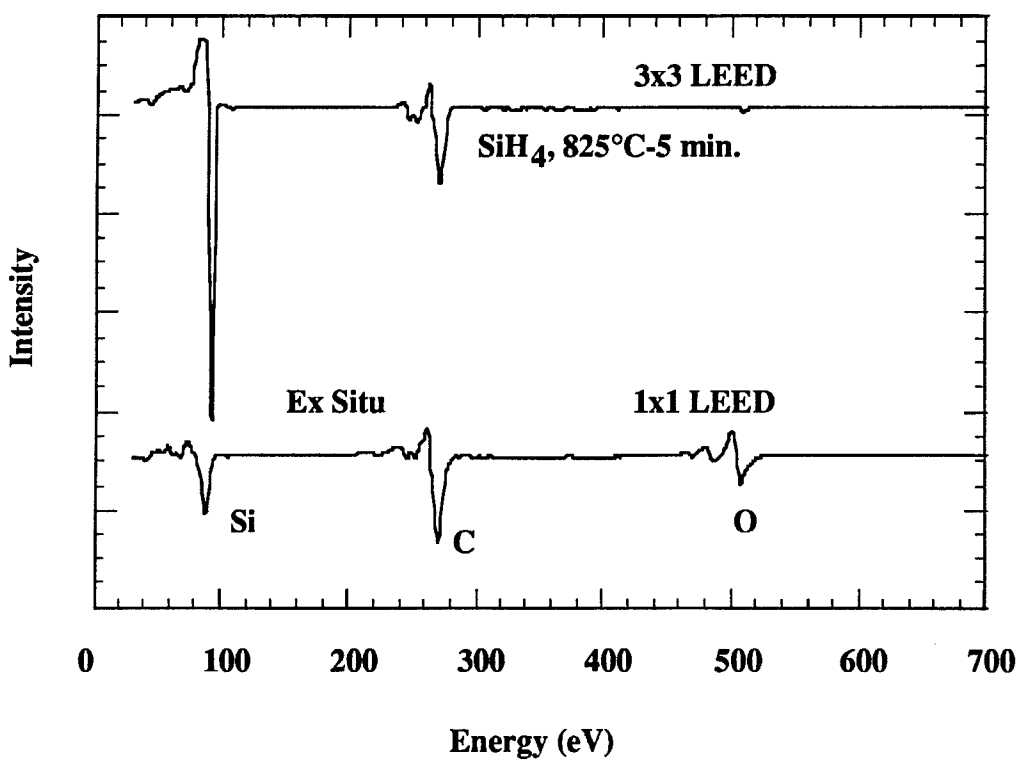

Figure 2. Silane CVD clean of 6H SiC.

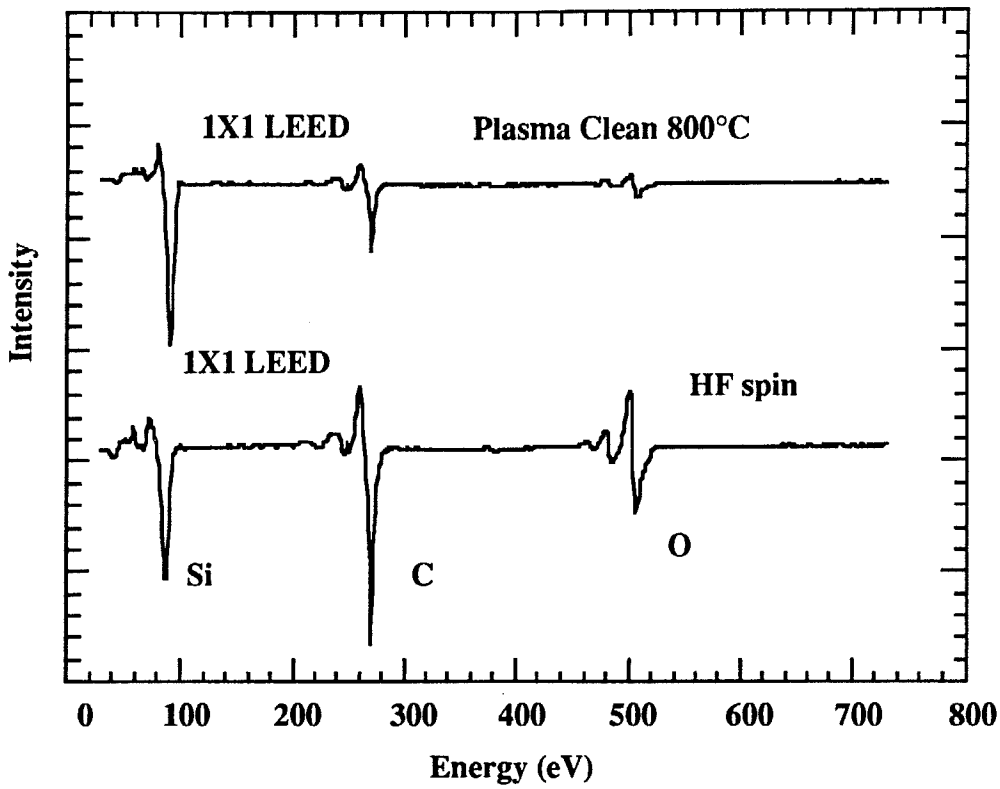

Figure 3. Remote silane plasma clean.

provide a source of 21.2 eV light. Photoemitted electrons are measured with a 50 mm mean radius hemispherical electron analyzer operated at a 0.15 eV energy resolution and a 2° angular resolution. The analyzer (VSW HA50) is mounted on a double goniometer and can be tilted with respect to the sample in two independent directions. The SiC samples were fastened by tantalum wire to a molybdenum sample holder. The sample holder is biased by up to 4 V to allow low energy electrons to overcome the work function of the analyzer. The Fermi level of the system (sample and analyzer) is determined by UPS measurement of the sample holder with no sample bias (i.e., grounded). The sample holder can be heated to 1150 °C.

Scans were performed on the CVD cleaned sample, a reconstructed sample and a hydrogen terminated clean sample. The reconstructed sample was the $\sqrt{3} \times \sqrt{3}$ R30° surface. This surface is prepared by annealing to 960 °C without a silane flow and is silicon deficient. The hydrogen terminated surface is a CVD cleaned sample which had a LEED pattern of 1×1. It was exposed to a hydrogen plasma to investigate the role of dangling bonds in the UPS spectra. The UPS data appears in Fig. 4.

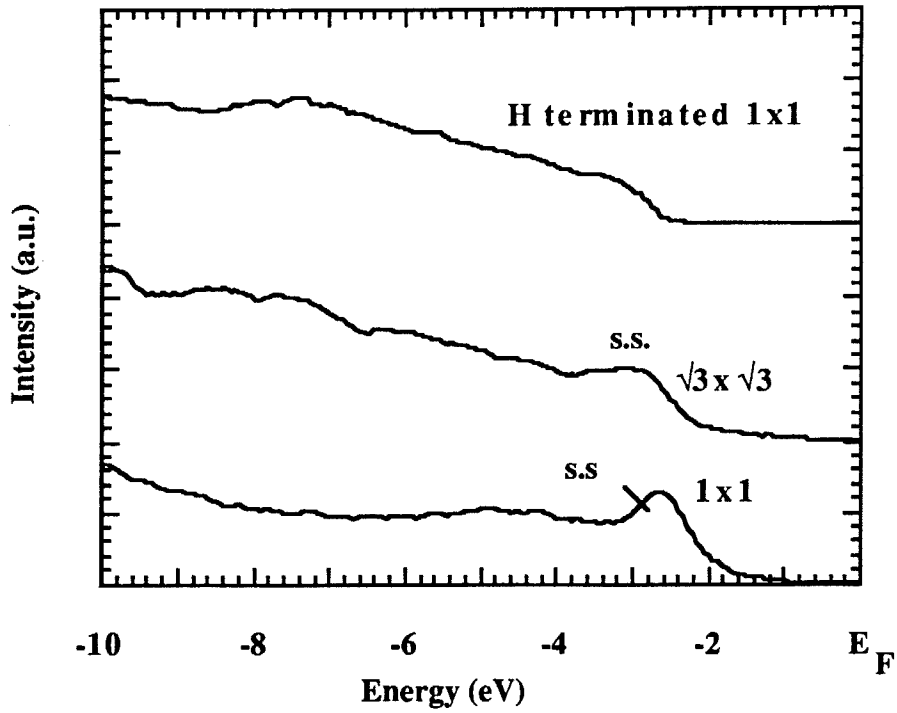

Figure 4. Surface states of SiC.

C. Results

The CVD clean removes substantial amounts of oxygen and hydrocarbons. We have an ordered surface with a 3×3 reconstruction. From the Auger spectra, we determine a Si/C ratio of 1.8 indicating a silicon rich surface. The LEED pattern is attributed to a Si adatom structure.

The plasma clean also removes contaminants yet gives us a 1×1 surface in registry with the bulk. The Si/C ratio is 1.2 so the surface is still slightly silicon rich.

The UPS investigation yielded very interesting results. We see a feature, a "bump," on the 1×1 surface which may be a surface state. The feature appeared diminished on a reconstructed surface. To test the origin of the state, we used the plasma system to terminate the surface with hydrogen. This resulted in the extinction of the feature. We attribute this extinction to the passivation of the surface. The dangling bonds are satisfied by the hydrogen atoms which terminate the surface.

D. Conclusions

We demonstrate cleaning of 6H SiC substrates by silane plasma and CVD methods. Currently we are unable to achieve the low temperature plasma clean which works so well for silicon. Yet, we have improved upon the pure chemical etch method. Lower processing temperatures are desired for industrial purposes. An advantage over silicon processing is that the temperature need not be as low, due to differences in diffusion of dopants.

We have made the observation of surface states on SiC. To our knowledge, this is the first report of such phenomena for SiC.

E. Future Plans

Refinement of the plasma processing parameters will be made with the goal being achievement of a lower processing temperature.

Further investigation of the surface state structure will be made by UPS. The 3×3 surface will be examined. This probe of the surface structure should lead to a better understanding of surface kinetics which in turn should help further develop the cleaning process.

F. Acknowledgment

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III. Growth of SiC Thin Films by Gas-Source Molecular Beam Epitaxy and Their Electrical Characterization

A. Introduction

Silicon carbide (SiC) is a wide bandgap material that exhibits polytypism, a one-dimensional polymorphism arising from the various possible stacking sequences of, e. g., the silicon and carbon layers along the directions of closest packing. There are approximately 250 SiC polytypes[1]. Included in these is one cubic polytype. This single cubic polytype, β-SiC, crystallizes in the zincblende structure, has a room temperature bandgap of 2.3 eV, and is commonly referred to as 3C-SiC. (In the Ramsdell notation, the three (3) refers to the number of Si and C bilayers necessary to produce a unit cell and the C indicates its cubic symmetry.) The other rhombohedral and hexagonal polytypes are classed under the heading of α-SiC. The most common of these latter polytypes is 6H-SiC with a room temperature bandgap of ≈ 3.0 eV.

Since the 1950's, monocrystalline single crystals of 6H-SiC have been grown at using the Lely sublimation process[2]. However, nucleation was uncontrolled using this process and control of resultant polytypes was difficult. SiC single crystals inadvertently formed during the industrial Acheson process have also been used as substrates for SiC growth. However, neither these nor those formed using the Lely process are large enough for practical device applications. Recently, using a seeded sublimation-growth process, boules of single polytype 6H-SiC of >1 inch diameter of much higher quality of that obtained using the Lely process have been grown. The use of single crystals of the 6H polytype cut from these boules has given a significant boost to SiC device development.

SiC epitaxial thin film growth on hexagonal SiC substrates has been reported since the 1960's. The use of nominally on-axis SiC substrates has usually resulted in growth of 3C-SiC films. Films of 3C-SiC(111) grown by CVD have been formed on 6H-SiC substrates less than 1° off (0001)[3]. Films of 3C-SiC on 6H-SiC substrates have typically had much lower defect densities than those grown on Si substrates. The major defects present in β-SiC/6H-SiC films have been double positioning boundaries (DPB)[4]. Despite the presence of DPBs, the resultant material was of sufficient quality to further device development of SiC. The use of off-axis 6H-SiC(0001) substrates has resulted in growth of high-quality monocrystalline 6H-SiC layers with very low defect densities[5].

In addition, the use of more advanced deposition techniques, such as molecular beam epitaxy (MBE), has been reported for SiC in order to reduce the growth temperature and from about 1400-1500°C on 6H-SiC substrates. Si and C electron-beam sources have been used to epitaxially deposit SiC on 6H-SiC (0001) at temperatures of 1150°C[6]. Previous reports by all investigators have documented 3C-SiC growth only on 6H-SiC(0001) by MBE.

B. Experimental Procedure

Thin, epitaxial films of SiC were grown on the Si and C faces of 6H-SiC(0001) substrates supplied by Cree Research, Inc. These included both vicinal 6H-SiC(0001) wafers oriented 3-4° towards [11$\bar{2}$0] containing a 0.75 μm epitaxial 6H-SiC layer deposited via CVD and on-axis 6H-SiC(0001) wafers. All wafers were received with a thermally oxidized 50 nm layer to aid in wafer cleaning. Wafers are prepared for growth by a 10% HF dip and a 10 minute anneal at 1050°C in UHV as well as a disilane exposure and boil-off, a technique detailed in previous reports and based on the work of Kaplan[8].

All films were grown using a specially designed and previously described [9] GSMBE system. The base and operating pressures were 10^{-9} Torr and 10^{-3}–10^{-6} Torr, respectively. All films were grown between 1050–1250°C using 1:1 ratios of disilane (Si_2H_6, 99.99% purity) and ethylene (C_2H_4, 99.99% purity) with total source inputs ranging from 0.6-4.0 sccm on off-axis α(6H)-SiC(0001) and thin 2H-AlN(0001) buffer layers on on-axis α(6H)-SiC(0001). The thin AlN layers were grown for 1 minute in the same system at 1050°C using a standard Al (99.9999% purity) effusion cell source, operating at 1260°C, and a compact electron cyclotron resonance (ECR) source to activate 3.5 sccm of N_2 (99.9995% purity). (This procedure has been described previously [10, 11]). As described in previous reports, both 3C- and 6H-SiC have been grown on vicinal a(6H)-SiC(0001) substrates depending on the chemistry of the gas phase and the substrate temperature. For the purposes of the doping studies, the 6H polytype was the only one investigated and only those films grown at 1250°C using 1.0 sccm Si_2H_6 and 1.0 sccm C_2H_4. Solid aluminum, evaporated from a standard MBE effusion cell, was used for p-type doping and ammonia (NH_3, diluted to 50 ppm in Ar) was used for p-type doping.

Reflection high-energy electron diffraction (RHEED) at 10 kV and high-resolution transmission electron microscopy (HRTEM) were used for structure and microstructure analyses. Samples were prepared for HRTEM using standard techniques[7]. A Topcon EM 002B high-resolution transmission electron microscope was used at 200 kV for the HRTEM analysis. Secondary ion mass spectrometry (SIMS), using a Cameca IMS-3f ion microprobe operating at 10 keV with O^+ ions, was employed to determine the atomic concentration of Al. Carrier concentrations for undoped SiC films, grown on insulating AlN layers, as well as p-type and n-type doped films were measured at room temperature by standard Hall techniques at 3.5 kG. Nickel contacts, RF sputtered at room temperature then annealed at 1000°C for 30 s in Ar, were used on the undoped and n-type films and aluminum contacts, evaporated in a standard evaporator and annealed at 500°C for 30 seconds in Ar, were used on p-type films.

C. Results

Undoped β-SiC Films. Undoped films of β-SiC(111) have been grown on thin, insulating layers of 2H-AlN(0001) at 1050°C using 1.0 sccm Si_2H_6 and 1.0 sccm C_2H_4. Growth rates

approaching 1000 Å per hour were achieved. Hall electrical measurements made on some of the thicker SiC films (≈0.75 μm) have showed the films to be n-type with electron concentrations as low as 3×10^{15} cm^{-3} and mobilities as high as 648 $cm^2V^{-1}s^{-1}$.

P-type Doping. Homoepitaxial SiC films on n-type substrates were doped p-type with Al at several different impurity concentrations. Carrier concentrations were measured on a number of Al-doped 6H-SiC films by the Hall technique. These films were grown under the previously stated conditions. Four different doping levels were achieved with Al effusion cell temperatures held at 700°C, 800°C, 900°C and 1000°C. The results are shown in Table I.

Table I. Hall Concentrations and Mobilities of Various P-type SiC Films

Aluminum Cell Temperature (°C)	Hole Concentration (cm^{-3})	Hole Mobility ($cm^2V^{-1}s^{-1}$)
700	4.6×10^{15}	39
800	7.1×10^{16}	33
900	8.8×10^{17}	26
1000	3.8×10^{18}	19

Figure 1 shows SIMS profiles for the same p-type films as displayed in Table I. Compared to our previously reported[12] p-type doped films, these profiles are very smooth and uniform.

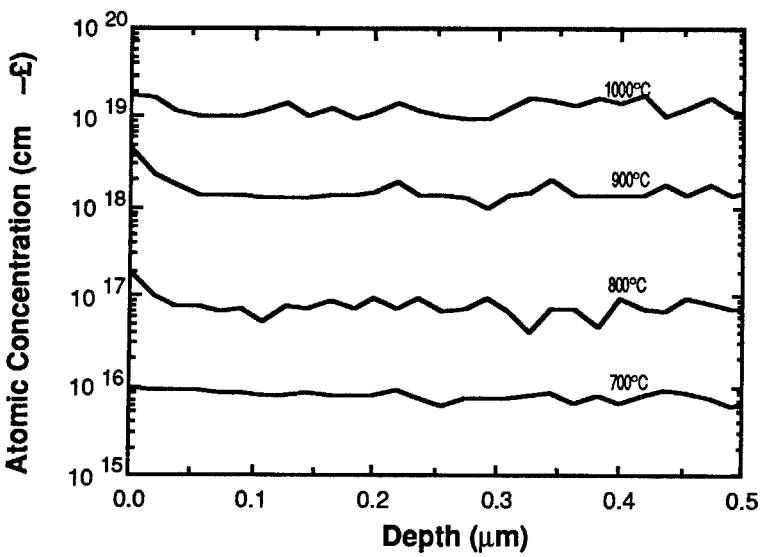

Figure 1. SIMS profiles for 6H-SiC films doped with Al from an MBE effusion cell at different source temperatures.

N-type Doping. Homoepitaxial SiC films on p-type substrates were doped n-type using NH_3, diluted to 50 ppm in Ar, at several different impurity concentrations. Carrier concentrations were measured on a number of N-doped 6H-SiC films by the Hall technique. These films were grown under the previously-stated conditions. Three different doping levels were achieved with NH_3/Ar flow rates at 0.33, 0.5 and 1.0 sccm. The results are shown in Table II. No SIMS analysis has been performed on these films.

Table II. Hall Concentrations and Mobilities of Various N-type SiC Films

NH3/Ar Flow Rate (sccm)	Electron Concentration (cm^{-3})	Electron Mobility ($cm^2V^{-1}s^{-1}$)
0.33	8.9×10^{16}	378
0.50	3.2×10^{17}	289
1.00	5.4×10^{17}	245

D. Discussion

The results of the Hall measurements on undoped β-SiC, grown on AlN on on-axis 6H-SiC, represent some of the lowest unintentional doping levels ever reported in the cubic polytype. The Hall measurements listed in Tables I and II and the SIMS data displayed in Fig. 1 represent the first intensive attempt at SiC doping ever attempted by MBE. As expected, the concentration of both impurity atoms and carriers increased as the source flux increased. The profiles in Fig. 1 and the data in Table I are of the same order of magnitude indicating a much higher activation efficiency in p-type SiC than previously reported by CVD [13]. In this case, the ratio of carrier concentration to impurity concentration is about 1 to 3. Unfortunately, the same data are currently unavailable on the n-type samples.

E. Conclusions

Films of 3C- and 6H-SiC have been grown between 1050-1250°C by GSMBE using Si_2H_6 and C_2H_4 on different orientations of α(6H)-SiC(0001) and on thin buffer layers of AlN. Growth of SiC on AlN represents a possible means of growing higher quality β-SiC(111) than previously reported. Hall electrical measurements on these films revealed carrier concentration as low as 3×10^{15} cm^{-3} and mobilities as high as 648 $cm^2V^{-1}s^{-1}$.

Doped films of 6H-SiC have been grown on vicinal α(6H)-SiC(0001) at 1250°C. The films (doped p-type with Al and n-type with N) showed carrier concentrations that increased

with increasing impurity flux. SIMS profiles for Al incorporation are of the same order of magnitude indicating a much higher activation efficiency than previously reported by CVD.

F. Future Research Plans and Goals

Further work on doping both 3C- and 6H-SiC will be performed. Simple device structures (i.e., p-n junctions) will be fabricated. Additionally, further studies will be initiated to study the role that hydrogen and other gases may play in the activation efficiency of carriers in SiC films. Since no hydrogen is used in MBE, aside from that released during the decomposition of the precursor gases, hydrogen incorporation is postulated[14] as a possible retardant to impurity activation. Experiments will be conducted with various levels of H_2 present to check the validity of this postulate.

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IV. Scanning Tunneling Microscopy of Vicinal and On-axis Surfaces of Epitaxial 6H-SiC (0001) Films

A. Introduction

Silicon carbide exists in >250 polytypes or stacking arrangements along the c-axis. The single cubic (zinc-blende) polytype is known as β- or 3C-SiC, where the 3 refers to the number of planes in the periodic sequence. The hexagonal (wurtzite) structure also occurs alone and in combination with 3C to form the remaining hexagonal or rhombohedral forms, known collectively as α-SiC, of which 6H is the most common. It has become an important semiconductor material because of its considerable potential for high-temperature, -power and -frequency device applications [1]. Homoepitaxial growth of 6H and 4H thin films is now commonly reported because of the availability of wafers of these polytypes. Chemical vapor deposition (CVD) is the primary process route (for a review of this work for SiC see Ref. [1]); however, molecular beam epitaxy (MBE) [2, 3] has also been used, as in the case of the present research. Films of 6H-SiC can be deposited via step flow mechanism on vicinal 6H-SiC (0001) surfaces as a result of the closely spaced steps which allow the retention of the same stacking sequence as the substrate [4, 5]. In contrast, the wider terraces on the surfaces of on-axis 6H material are unfavorable for sufficient mass transport to the steps for step flow growth. Instead, the terraces become the areas on which occur the nucleation and growth of islands of the 3C polytype [5]. The 6H substrates are also being increasingly used for the epitaxial growth of AlN and GaN due to the small mismatches in lattice parameters relative to most other available substrates [6, 7]. The defect density observed in AlN films has been shown to be sensitive to the 6H surface structure [8]. As such, knowledge of the step/terrace configuration and surface reconstruction on 6H-SiC substrates is important, as they determine film characteristics as well as surface chemistries.

Low energy electron diffraction (LEED) has been employed to determine the surface reconstruction on 6H(0001) and 3C(001) surfaces as a function of temperature [see, e.g., Refs. [9, 10]. Ultra high vacuum scanning tunneling microscopy (UHV-STM) has been used to investigate both 3C(111) films deposited via CVD on 6H-SiC(0001) [11] and the C-terminated surfaces of bulk crystals derived via sublimation (Lely process) [12].

In this study we have observed for the first time via UHV STM both the vicinal (~3.5° off 6H-SiC(0001) towards $<11\bar{2}0>$)) and on-axis, Si-terminated surfaces of 6H-SiC(0001) epitaxial layers having a thickness and donor carrier concentration of ~750 Å and ~6×10^{17}cm^{-3}, respectively, and grown commercially by CVD on 6H-SiC(0001) substrates. Each layer contained an ~1.5 μm thick thermally grown SiO_2 layer which acted both to remove the thin layer of C-containing material frequently present on the SiC film surface following the CVD process and to protect this surface prior to observation.

B. Experimental

The oxide layer was removed prior to loading using a 10 % HF solution for 5-8 min. To obtain clean surfaces, the sample was desorbed at 400-550 °C for 2-14 hrs and annealed at 1000-1250 °C for 3-5 min. in an Omicron 1 STM chamber. The sample temperature was monitored using an optical pyrometer. The STM study was performed at room temperature. Tungsten tips and a tunneling current and bias of 0.3 nA and -3.5 V, respectively, were used to image the surface.

C. Results and Discussion

Observations of the vicinal surface after annealing at 1150 °C for 3 min. revealed a strongly undulating step/terrace configuration, as shown in Fig. 1. Similar morphological features have been observed on GaAs film surfaces grown by metalorganic vapor phase epitaxy (MOVPE) at a relatively lower growth temperature compared to normal GaAs deposition temperatures [13]. Increasing the growth temperature of the latter material resulted in smoother step edges. It is

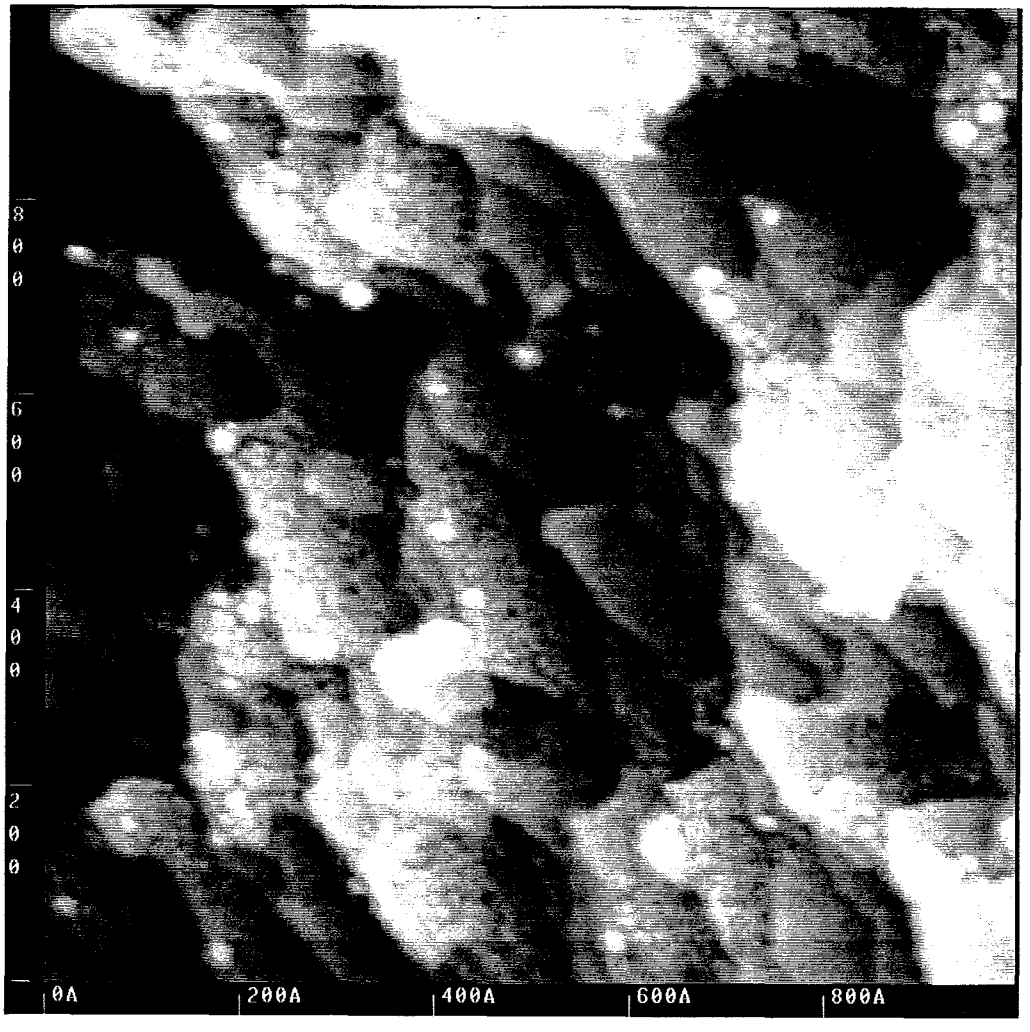

Figure 1. Surface feature of the vicinal 6H-SiC.

believed that the undulating step features are a result of insufficient surface diffusion lengths of adatoms. A honeycomb-like microstructure and contamination (white spots) were also observed on some terraces (see Fig. 1). The spots are believed to be residual silicon oxide which was not removed during the cleaning procedure. The cause of the honeycomb-like features will be discussed below in conjunction with surface chemistry. Most step heights were ~2.5 Å corresponding to single bilayer steps consisting of one Si and one C layer. The (1×1) hexagonal surface crystallography could not be resolved using the imaging parameters of this study.

Relatively wider terraces separated primarily by single bilayer steps were observed on the on-axis surface of a sample after annealing at 1000 °C for 3 min. in UHV, as shown in Fig. 2. In general, the steps descend along the direction, possibly as a result of step flow growth of the epitaxial layer. Some terraces, contain single bilayer deep holes (black region), similar to the feature shown in 6H-SiC, in reference [12] as well as islands (white region) of SiC. No honeycomb-like features were observed.

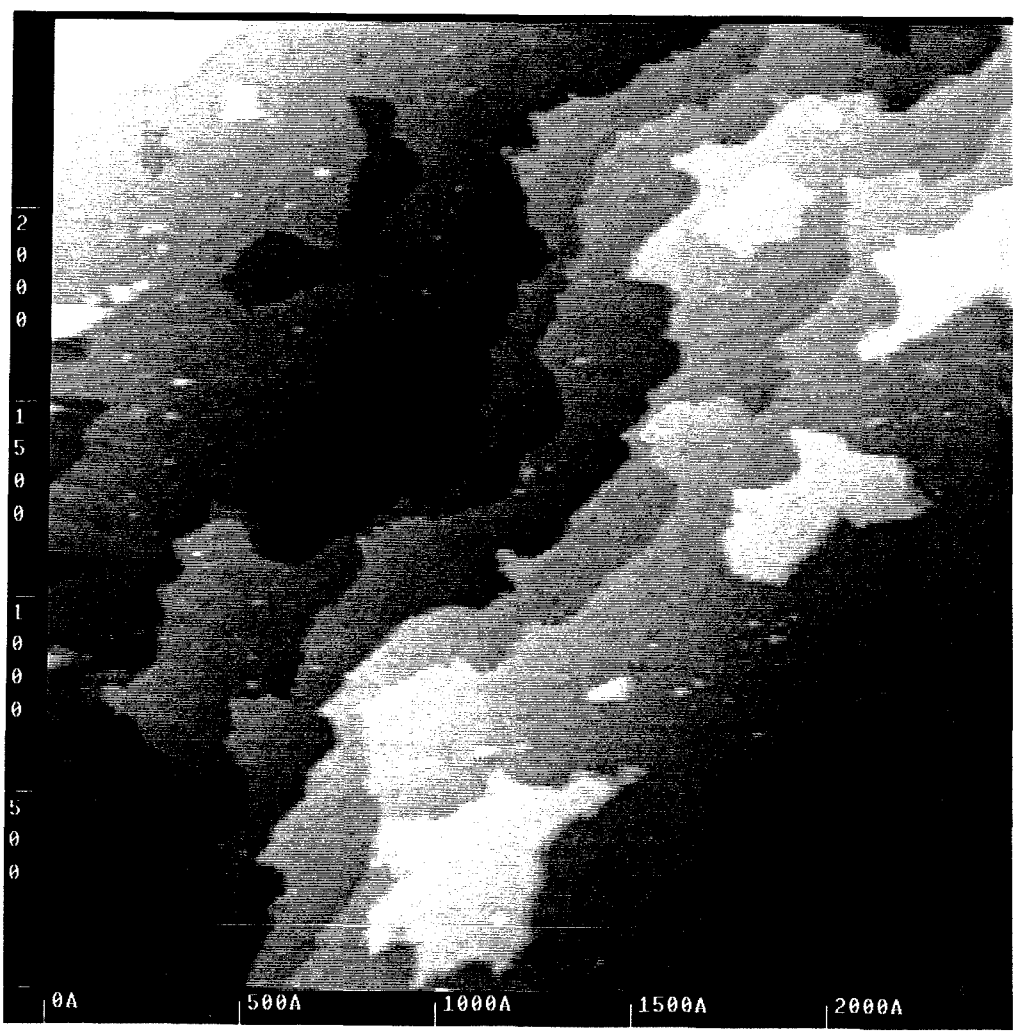

Figure 2. Surface feature of the on-axis 6H-SiC.

Figure 3 shows a high magnification image of a honeycomb-like feature observed on the on-axis terrace region after sequential annealing at 1000 °C and 1100 °C for 3 min. at each temperature in UHV. The unit cell of this structure was measured to be ~18.5 Å. According to surface chemical studies on 6H-SiC(0001) by Auger electron spectroscopy (AES), surface graphitization begins to occur above 1027 °C [14]. A model of a graphite monolayer has been proposed by Chang, et al. [11] based on their STM observations, which is in agreement with the aforementioned AES analysis and our results. Therefore, the honey-comb-like structure is very likely the result of surface graphitization due to Si sublimation during annealing.

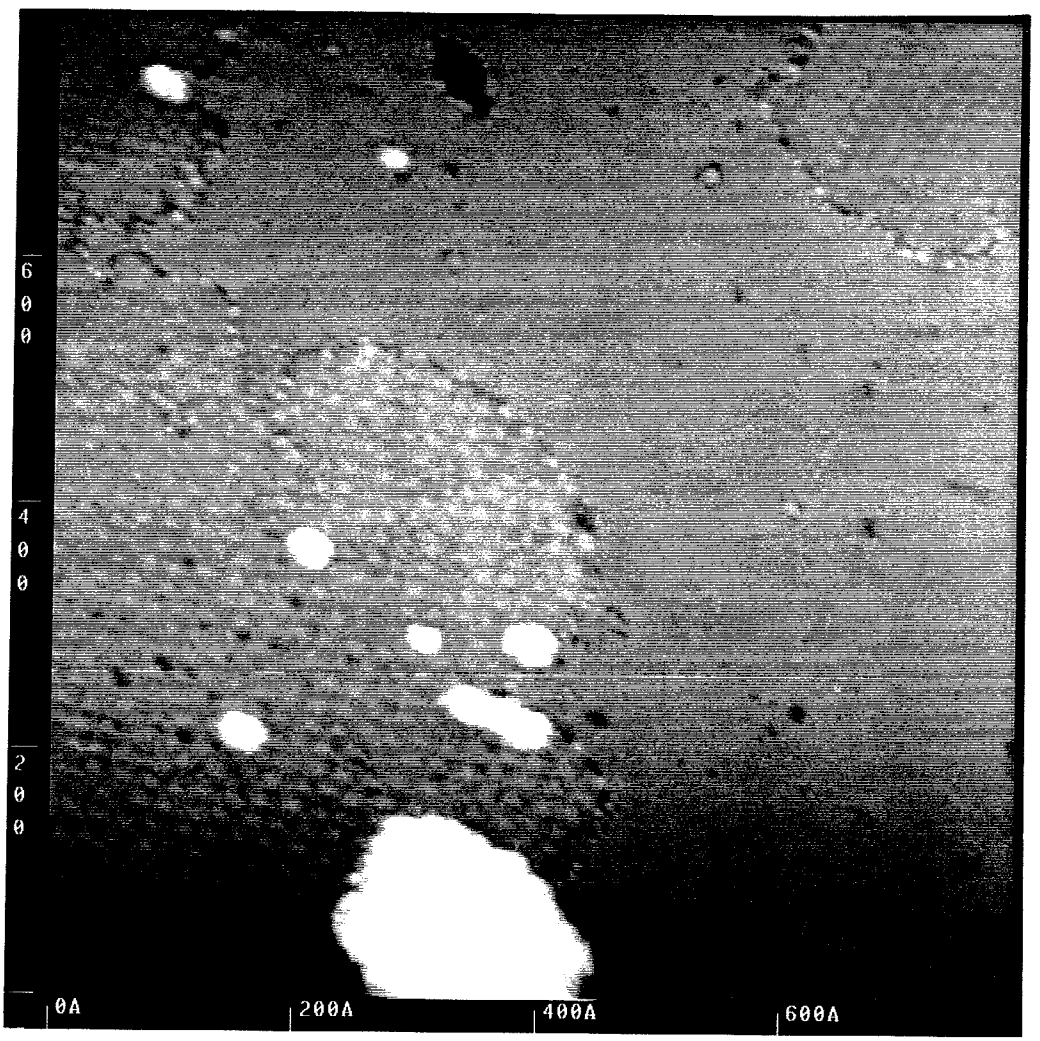

Figure 3. Honeycomb-like structure observed in the on-axis 6H-SiC substrate after annealed at 1100 °C

D. Conclusions

In summary, STM observations on the Si face of homoepitaxial layers deposited on commercially available vicinal and on-axis 6H-SiC(0001) wafers has been performed. A

strongly undulating step/terrace configuration was observed in the vicinal surface. By contrast, relatively wide terraces were observed on the on-axis surface. Single Si/C bilayer steps were dominant on both surfaces. A surface phase transformation due to Si sublimation from the Si-terminated surface and resultant graphitization during the cleaning procedure at T≥1100°C, were observed in both vicinal and on-axis surfaces. The effects of surface structures on both thin film growth by molecular beam epitaxy and defect formation will be published in the near future.

E. Future Research

The 6H-SiC wafers which have no epitaxial layer, as grown wafers, will be examined by the similar technique used in this study. In addition, the surfaces of the epitaxial layers grown in our GSMBE system will be investigated in terms of occurrence of step bunching and step flow. It is also interesting to investigate the atomistic structure of the step in 6H-SiC surfaces by a higher resolution STM.

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V. Chemistry, Microstructure, and Electrical Properties at Interfaces Between Thin Films of Platinum and Alpha (6H) Silicon Carbide (0001)

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Abstract

Thin films (4–1000Å) of Pt were deposited via UHV electron beam evaporation at room temperature on monocrystalline, n-type α (6H)-SiC (0001) substrates and examined in terms of chemistry, microstructure, and electrical properties. The as-deposited contacts were polycrystalline and showed excellent rectifying behavior with low ideality factors ($n < 1.1$) and leakage currents of 5×10^{-8} A/cm^2 at -10 V. The Schottky barrier height increased from 1.06 eV before annealing to 1.26 eV after successive 20 min. anneals at 450, 550, 650, and 750°C. In addition, the leakage currents decreased to 2×10^{-8} A/cm^2 at -10 V. Interfacial reactions were not observed at annealing temperatures below 750°C; above this temperature, which Pt_2Si and C precipitates were identified in the reaction zone.

A. Introduction

The high strength and extreme thermal and electronic properties of SiC coupled with the high melting point, high work function, and metallic properties of Pt have led to interest in the Pt/SiC system for both structural and electronic applications. Chou [1] investigated Pt/SiC diffusion couples (1-2 mm thick) for ceramic reinforced metal composites. Similar to the results in the present study, both Pt silicides and free C were identified in the reaction zones after annealing at temperatures between 900 and 1000°C. An extension of this work [2] showed the presence of several silicides after annealing at 1100°C ≤ 4 h. In contrast to the present research in which thin films (≤1000Å) were used, annealing the thick Pt/SiC samples at high temperatures resulted in the formation of alternating silicide and C layers. Significant differences in the product phases are often observed for annealed thick and thin films of Pt on SiC particularly if the thin films are completely consumed.

The interfacial chemistry and structure of ultrathin (≤8Å) films of Pt deposited on β-SiC (001) were studied by Auger electron spectroscopy (AES) and low energy electron diffraction (LEED).[3] The results indicated no chemical reaction after annealing for 10 s at 800–900°C and silicide and graphite formation after annealing for 10 s at 1000°C.

Papanicolaou *et al.* [4] studied the electrical characteristics of Pt on n-type β-SiC annealed for 20 min. at temperatures between 300 and 800°C. The study showed that Pt was a good Schottky contact with a high Schottky barrier (0.95–1.35 eV) throughout the annealing sequence. However, the reverse current densities were at least six orders of magnitude higher than those observed in the present study. The higher reverse currents are likely due to a higher defect density in the β-SiC films than in the 6H-SiC substrates and/or the difference in surface preparation. High voltage Pt Schottky barrier diodes have been fabricated on n-type 6H-SiC at 140°C.[5] The as-deposited diodes displayed a high breakdown voltage (>425 V), a low forward voltage drop, low leakage currents, and excellent switching characteristics.

While there have been a number of studies of the Pt/SiC interface highlighting its potential applications, this is the first to correlate the electrical, chemical, and microstructural properties between thin Pt films (≤1000Å) and semiconductor quality 6H-SiC as a function of annealing. In this study analytical techniques, including high resolution transmission electron microscopy (HRTEM), x-ray photoelectron spectroscopy (XPS), and current-voltage (I-V) measurements, were used to understand the chemistry, microstructure, and electronics at interfaces between Pt and monocrystalline, n-type α(6H)-SiC (0001) substrates. These properties were examined for both as-deposited interfaces and after annealing between 450 and 750°C. The Schottky barrier height (SBH), a critical property for determining the electrical properties, was also calculated through the annealing series.

B. Experimental Procedure

Vicinal, single crystal, nitrogen-doped, n-type ($\approx 10^{18}$ cm^{-3}) wafers of 1" diameter α (6H)-SiC (0001) containing 0.5-1.5 μm thick, unintentionally doped n-type ($\approx 10^{16}$–10^{17} cm^{-3}) homoepitaxial films thermally oxidized to a thickness of 500-1000Å in dry oxygen at 1300°C were provided by Cree Research, Inc. Epitaxial layers, intentionally doped with nitrogen during growth to achieve an n-type carrier concentration of $\approx 2\times10^{18}$ cm^{-3}, were also employed in this research. The Si-terminated (0001) surface, tilted 3°-4° towards [11$\bar{2}$0] was used for all depositions and analyses.

The substrates were simultaneously cleaned and the oxide layer etched from the surface using a 10 min. dip in a 10% hydrofluoric acid solution. This was followed by a quick rinse in deionized water. The substrates were loaded immediately into a vacuum system transfer tube (base pressure $\approx 10^{-9}$ Torr), thermally desorbed at 700°C for 15 min. to remove any residual hydrocarbon contamination, and transferred to the metal deposition chamber.

A UHV dual source 270°, 10 cc electron beam evaporation system was used to deposit the Pt films having thicknesses ranging from 4 - 1000 Å onto the substrates described above. A 330 l/s turbomolecular pump was used for roughing the system and during processing. A 500 l/s diode ion pump and a Ti sublimation pump were employed to achieve and maintain UHV base pressures of $<2\times10^{-10}$ Torr. Prior to the depositions, approximately 25–50 Å was typically evaporated from the source to liberate any foreign material which may have collected on its surface. Each substrate was covered by a shutter during this operation. To commence the deposition, the emission current was increased very slowly until a deposition rate of 10–12 Å/min was stabilized according to the thickness monitor, and the shutter subsequently removed from in front of the sample. The pressure during the depositions was between 5×10^{-9} and 5×10^{-8} Torr. Throughout each deposition the substrates were rotated to ensure uniform thickness across the sample. The substrates were not intentionally heated during the depositions.

Patterned contact structures consisting of 500 μm (0.02") and 750 μm (0.03") diameter circular contacts of 100 nm thickness were created for electrical characterization by depositing the Pt through a Mo mask in contact with the SiC epitaxial layer. Silver paste served as the large area back contact. All subsequent annealing, which consisted of successive heating at 450, 550, 650, and 750°C for 20 min. at each temperature, was conducted in UHV. Current-voltage (I-V) measurements were taken with a Rucker & Kolls Model 260 probe station in tandem with an HP 4145A Semiconductor Parameter Analyzer.

Pt/SiC samples were prepared in cross-section for analysis by TEM. High resolution images were obtained with an ISI EM 002B operating at 200 kV with an interpretable resolution limit of 0.18 nm. These images were typically recorded at an electron-optical magnification of 490,000 to 590,000. Some of the HRTEM micrographs were digitized using a 512×512 camera and the resulting images analyzed by using the SEMPER program.[6] Lattice spacings (d-spacings) and interplanar angles were measured from optical digital diffraction patterns and used to identify the reaction product phases. The values of the lattice spacings were calculated using the (0006) d-spacing in 6H-SiC as a baseline measured near the phase to be identified. Thus, any change in d-spacing due to different focusing conditions was negated. A data base of d-spacings for each possible reaction product phase was compared to the experimentally-determined values. The d-spacings from the data base which were within 2% of the measured values were compared with interplanar angles for the identification of phases. Most of the measured values were within 1% of the theoretical values. Unknown phases were identified uniquely by these procedures.

Analytical electron microscopy was performed using a Gatan 666 parallel electron energy loss spectrometer (PEELS) with a spatial resolution of approximately 3 nm attached to a Philips 400 FEG operating at 100 kV . Energy dispersive spectrometry (EDS) was performed using a JEOL 2000 FX operating at 200 kV with a probe size of approximately 40 nm. For fixed position PEELS and EDS, the probe position was adjusted in the diffraction mode by monitoring the shadow image in the Bragg disk of the transmitted beam. The image was created by defocusing the second condenser lens. A liquid nitrogen cooled double-tilt holder was used for all analytical experiments to minimize specimen contamination.

The surface and interface chemistry of the Pt/SiC assembly were studied using a Riber XPS system containing a Mac2 semi-dispersive electron energy analyzer and accessible by UHV transfer from the deposition chamber. The Mg Kα (1253.6 eV) x-ray source was operated at 14 kV with an emission-controlled current of 15 mA. Scans of individual photoelectron peaks were obtained at 0.8 eV resolution and contained 500-750 data points and a 20-30 eV binding energy range. This technique also allowed the calculation of the Schottky barrier height for thin films of Pt on SiC.

C. Results and Discussion

Electrical Properties. Platinum contacts displayed excellent and very stable rectifying characteristics both in the as-deposited state and after successive 20 min. anneals at 450, 550, 650, and 750°C. Before annealing, the leakage currents and ideality factors were typically $5 - 10\times10^{-8}$ A/cm^2 and n<1.1, respectively. An I vs. V plot which is representative of the results after each successive stage of the annealing series is shown in Fig. 1. Leakage currents at -10 V of the annealed samples were 2×10^{-8} A/cm^2.

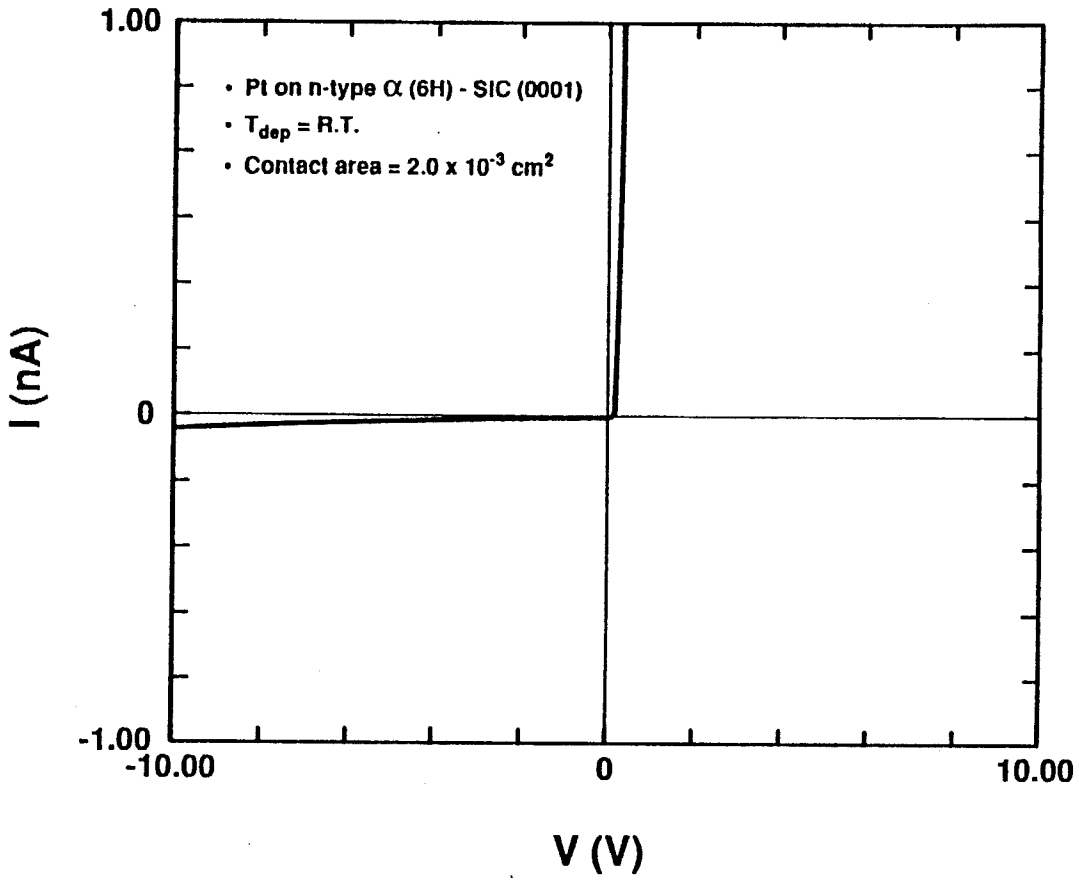

Figure 1. Representative current vs. voltage measurement for Pt/SiC contact after successive annealings for 20 min. at 450, 550, 650, and 750°C.

The semilogarithmic plot of I vs. V in Fig. 2 shows that the characteristics maintained the same slope (and, therefore, ideality factor) but shifted to a higher voltage with each successive anneal. Calculations based on these results show that the SBH increased from 1.06 eV for the as-deposited contacts to 1.26 eV after annealing at 750°C, as presented in graphical form in Fig. 3. These results are similar to those reported by Papanicolaou et al.[4] in which the SBH of Pt on β-SiC (001) increased steadily after annealing for 20 min. each at 450, 600, 700, and 800°C. The SBH was 0.95 eV for as-deposited contacts and 1.35 eV after annealing at 800°C.

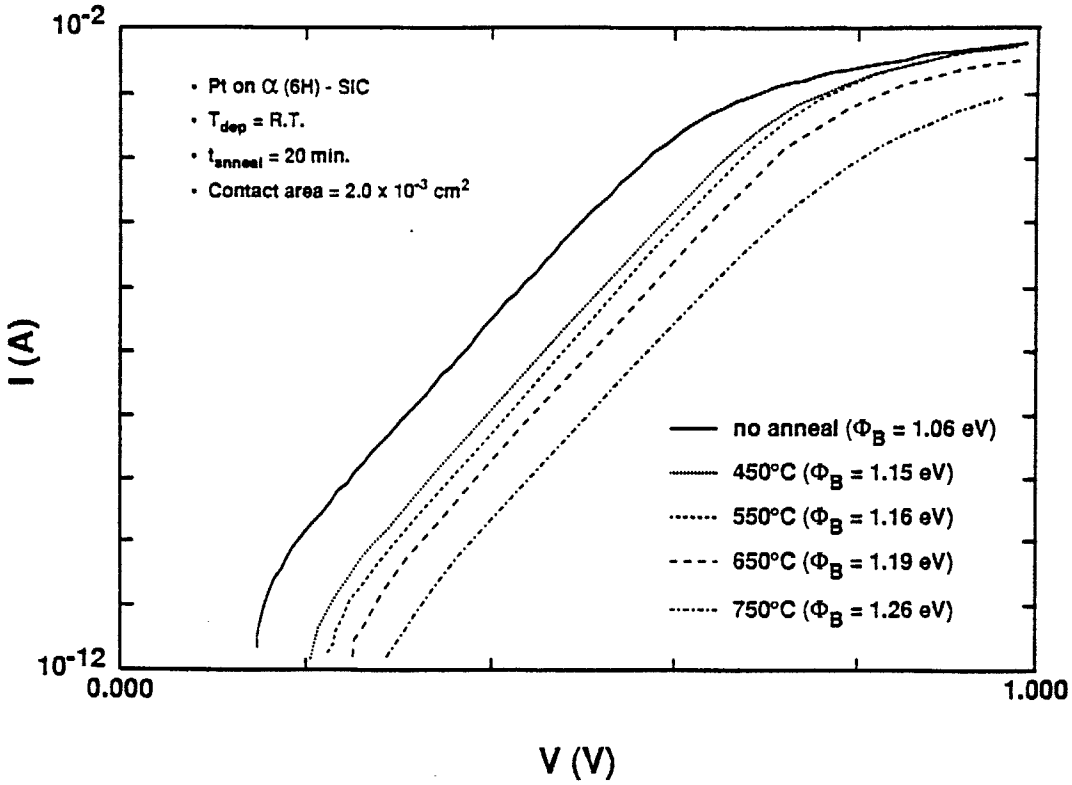

Figure 2. Semilogarithmic current vs. voltage plot for as-deposited Pt/SiC through successive annealing series at 450, 550, 650, and 750°C for 20 min. at each temperature.

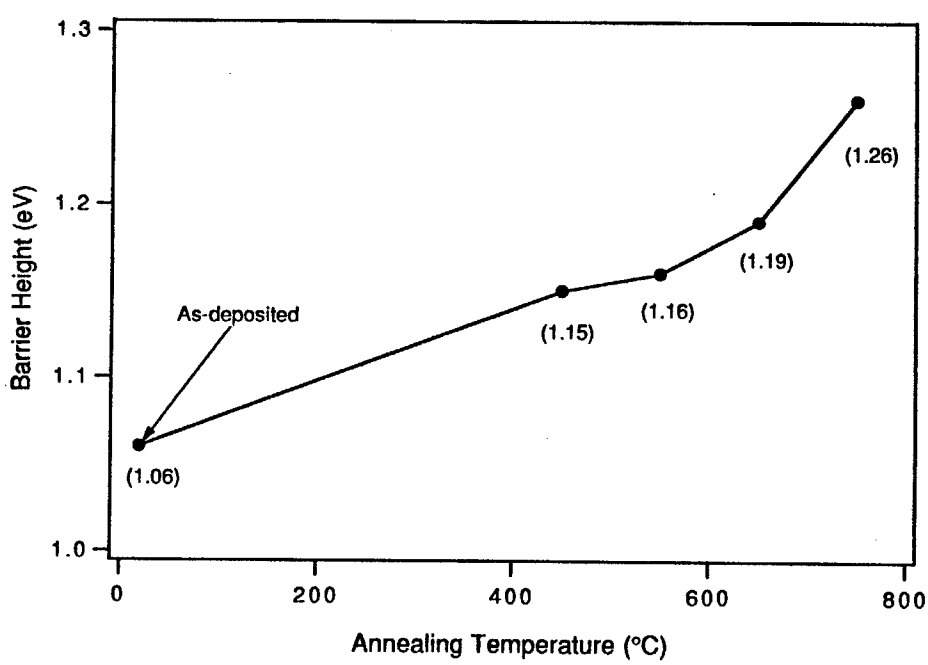

Figure 3. Schottky barrier heights of Pt/SiC vs. annealing temperature.

The SBH was also calculated for very thin, as-deposited Pt films from XPS data using the method described in Ref. 7. The Si 2p and C 1s peaks were used to determine the amount of band bending at the SiC surface/interface before and after deposition. Table I lists the binding energies of these peaks.

Table I. Binding energies of Si 2p (Si-bound-to-C) and C 1s (C-bound-to-Si) peaks from SiC with various thicknesses of Pt. These binding energies have been corrected according to the Au $4f_{7/2}$ binding energy. Units are in electron-volts.

Peak	0 Å Pt	4 Å Pt	8 Å Pt	12 Å Pt
Si 2p	101.58	101.32	101.24	100.64
C 1s	283.80	283.56	283.50	282.96

It is important to assure complete coverage by the Pt films after the depositions. The growth mode was examined following the procedure outlined in Ref. 7. For Pt, which is fcc (a = 3.92 Å), one monolayer was taken to be 2.26 Å. The calculated C 1s and Si 2p reduced intensities are plotted vs. Pt thickness in Fig. 4. The measured intensities attenuated more

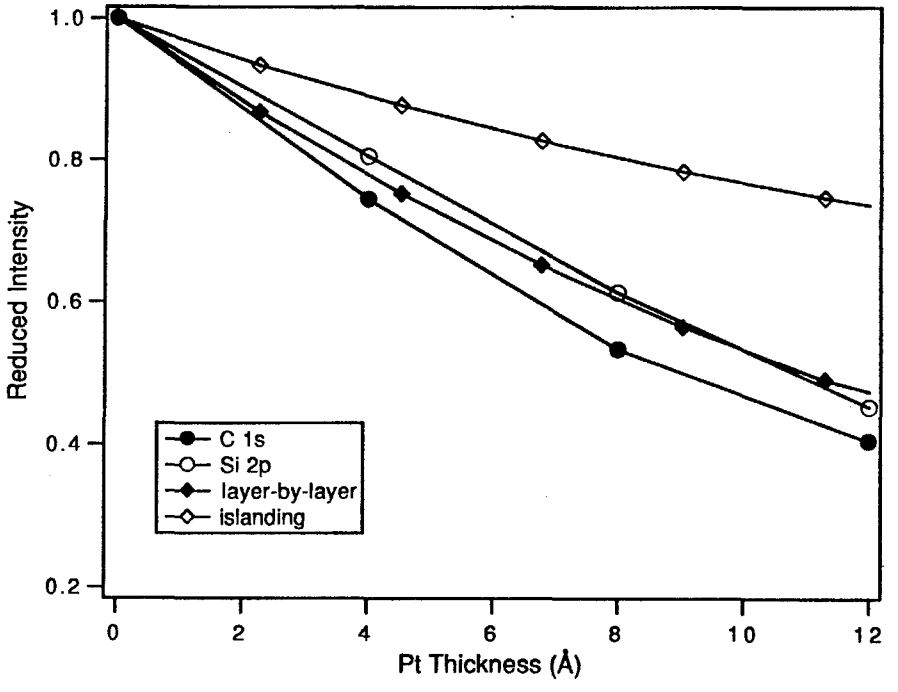

Figure 4. Plot of C 1s and Si 2p reduced intensities vs. Pt overlayer thickness as measured by the growth thickness monitor. The theoretical curves represent two-dimensional layer-by-layer (Frank van der Merwe) and three-dimensional island (Volmer-Weber) growth.

rapidly than the theoretical curve for three-dimensional, or island, growth (assuming 50% coverage). Less attenuation of the substrate intensities is expected for island growth because some regions of the substrate are not covered by the deposited film. The data is shown to follow the theoretical curve for two-dimensional, or layer-by-layer, growth, indicating complete coverage of the SiC substrate by the Pt film.

The C 1s and Si 2p peaks for a Pt deposition sequence are displayed in Fig. 5. The band bending at the SiC surface prior to deposition was determined from the C 1s binding energy. Subtracting the C 1s binding energy of 283.80 eV from 284.30 eV (see Ref. 7) indicates that the energy difference between the bottom of the conduction band and the Fermi level was 0.50 eV. After depositing 4 Å of Pt the C 1s and Si 2p binding energies were reduced by 0.24 and 0.26 eV, respectively. After depositing a total of 12 Å, these binding energies were reduced by a total of 0.84 and 0.82 eV, respectively.

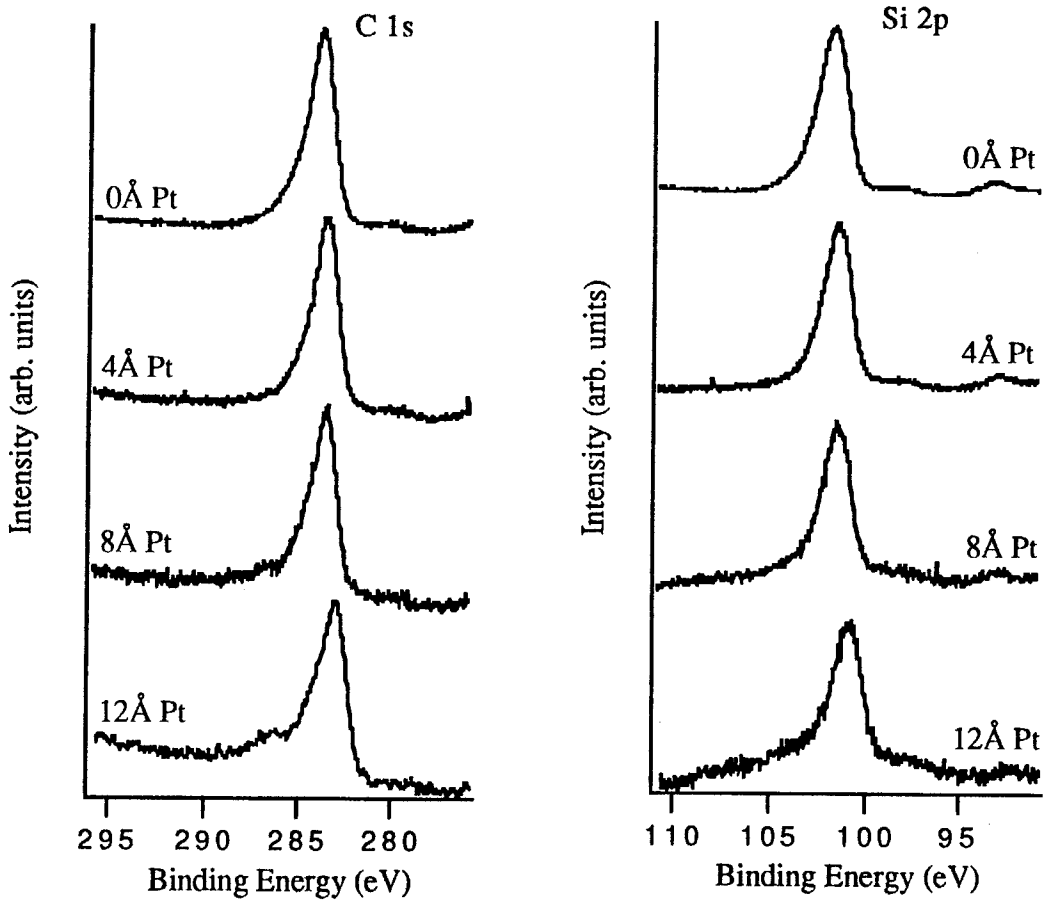

Figure 5. XPS C 1s and Si 2p photoelectron peaks from SiC (0001) before and after deposition of 4, 8, ans 12 Å of Pt.

The possibility that the decreasing binding energies with increasing metal overlayer thickness was a result of a corresponding decrease in sample charging was considered. However, the amount of change in the binding energies as shown in Table I was much larger than the corresponding differences found in clean SiC surfaces, the latter of which were attributed to sample charging. Thus, the results indicate that most of the binding energy changes can be attributed to both increasing coverage and charge transfer from thicker Pt layers. Comparison of the XPS data to the I-V measurements indicates that films thicker than 12 Å should not cause significant, additional changes in the barrier height. Taking the average of the binding energy reductions and adding it to the initial amount of band bending gives a barrier height of 1.33 ±0.1 eV. This calculated value is 0.27 eV higher than the value calculated from I-V measurements. The possible reason for this discrepency will be discussed in the following section.

Microstructure. Transmission electron microscopy analysis showed that the as-deposited Pt films were random polycrystalline with grain sizes of 10 ± 3 nm (Fig. 6). As the annealing temperature was increased from 450 to 650°C, the $[111]_{Pt} \parallel [0001]_{SiC}$ oriented grains grew at the expense of the other grains. The average grain sizes after annealing at 550 and 650°C were 40 and 65 nm, respectively. The increase in grain size may be observed by comparing Fig. 7, which shows a cross-sectional TEM micrograph of a sample annealed at 650°C, to Fig. 6. No evidence of an interface reaction zone was observed via HRTEM in any of the samples annealed at or below 650°C; however, a limited amount of interdiffusion was detected in the samples annealed at 650°C. Platinum had diffused several nanometers into the SiC at some localized regions. Some steps a few nanometers thick were also observed at the interface. The crystallographic relationships between Pt and SiC in these latter samples were determined from SAD patterns of a sample in cross-section:

$$[011]_{Pt} \parallel [11\bar{2}0]_{SiC}$$

$$(111)_{Pt} \parallel (0001)_{SiC}$$

$$[111]_{Pt} \parallel [0001]_{SiC}$$

$$(220)_{Pt} \parallel (11\bar{2}0)_{SiC}.$$

The mismatch between Pt and SiC was $\{|d_{(220)Pt} - d_{(11\bar{2}0)SiC}| \div d_{(11\bar{2}0)SiC}\} \times 100\% = 9.70\%$. Although this mismatch is not small, the mismatches between other low index crystal planes of Pt and SiC are even higher. Table II lists the calculated lattice mismatches between some of the low index crystal planes. These results indicate that the preferential grain growth with annealing occurred in order to decrease the strain associated with the interface.

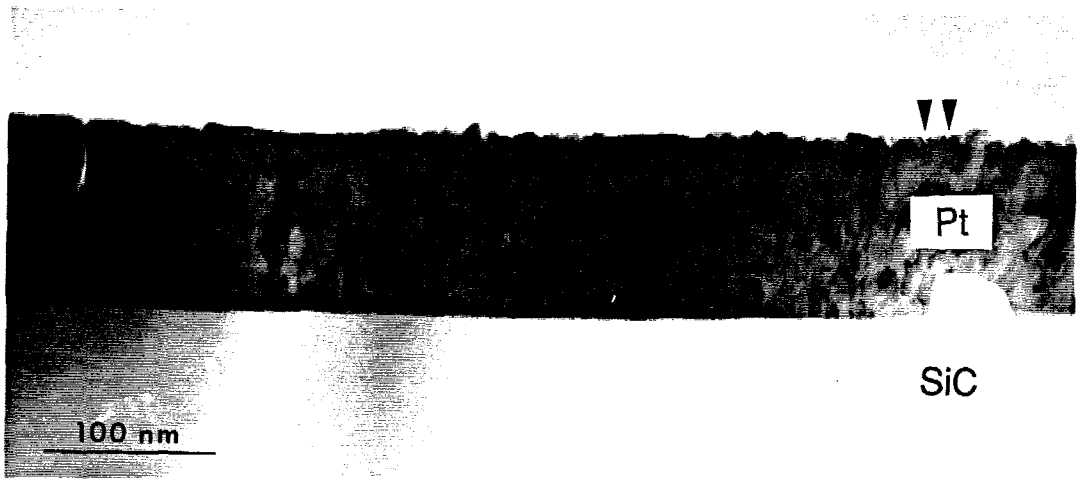

Figure 6. Cross-sectional TEM image of Pt deposited at room temperature onto 6H-SiC (0001). The average grain size of the Pt film was 10 nm.

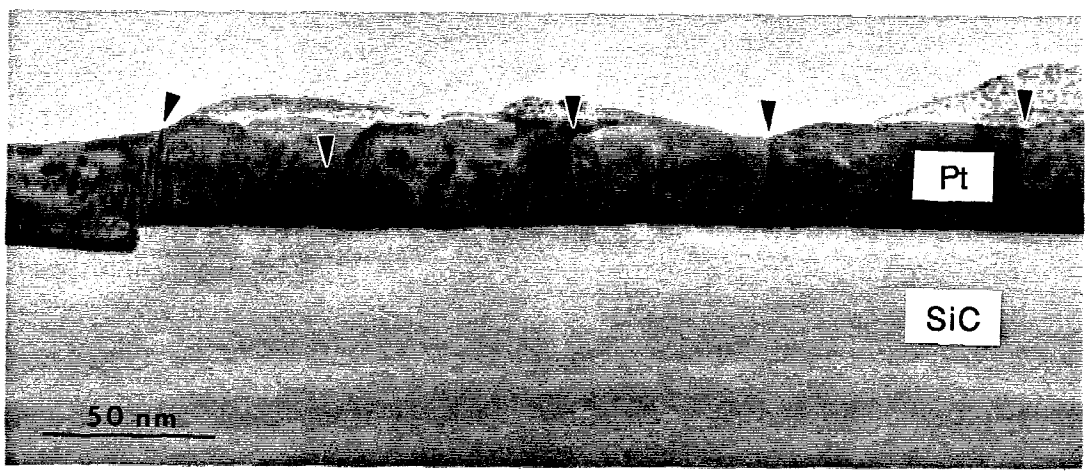

Figure 7. Cross-sectional TEM image of Pt/SiC annealed at 650°C for 20 min. The arrows delineate the grain boundaries. The average grain size of the Pt film was 65 nm.

The evolution in the preferred orientation of the Pt grains noted above may be correlated with the increasing SBH determined via I-V measurements as a function of annealing temperature to 650°C (Fig. 3) by comparing SBH's determined from XPS and I-V measurements. The smaller value calculated for the as-deposited sample from the latter technique is likely due to inhomogeneities at the polycrystalline metal-semiconductor interface produced by the variety of grain orientations, interfacial strain, defects, and/or trace O (~3 at. %) detected at the the interface by PEELS. The microstructural inhomogeneities are believed to cause variations in the SBH as a function of position along the interface.

Table II. Calculated lattice mismatches between low index planes in Pt and 6H-SiC.

(h k i l)SiC	d-spacing (Å)	(h k l)Pt	d-spacing (Å)	mismatch (%)
$(1\bar{1}00)$	2.661	(111)	2.2650	14.88
$(1\bar{1}00)$	2.661	(200)	1.9616	26.28
$(1\bar{1}00)$	2.661	(220)	1.3875	47.86
$(11\bar{2}0)$	1.5365	(111)	2.2650	47.41
$(11\bar{2}0)$	1.5365	(200)	1.9616	27.67
$(11\bar{2}0)$	1.5365	(220)	1.3875	9.70

Current-transport at inhomogeneous interfaces is dominated by the regions with the lowest SBH, which results in calculated SBH's from I-V measurements which are lower than the arithmetic average of the entire interface.[8-13] This phenomenon would explain why the SBH calculated from I-V measurements was 0.27 eV lower than that calculated from XPS analyses, the latter of which should yield a value closer to the average value. While capacitance-voltage measurements should also yield a value closer to the average SBH, the results were bias dependent and somewhat erratic, a result which also may be due to the resulting microstructure.

Both the randomness of the grain orientations and the interfacial O decreased after annealing. This change was accompanied by and directly correlated with an increase in the SBH calculated from I-V measurements.

Interfaces along which the SBH varies usually are associated with ideality factors which are bias dependent; however, interfaces which contain a distribution of low SBH areas, as opposed to one large area, display much less dependence of the ideality factor on bias.[13] Bias dependence of the ideality factors was not found for the Pt contacts below voltages at which the current became limited by the resistance of the SiC. The Pt contacts before and after annealing displayed low ideality factors over three to four decades of current. The electrical properties, along with the observation of the small grain size in the Pt films, indicate that inhomogeneities in microstructure and SBH exist and are finely-dispersed throughout the interface.

Chemistry. The annealed Pt/SiC interfacial chemistry has been investigated with high resolution TEM and its associated analysis techniques. After annealing at 750°C for 20 min., a 45 nm thick reaction zone formed as shown in Fig. 8. This zone was composed of an amorphous, irregular-shaped, white phase layer of C and a dark, crystalline Pt_2Si phase. Parallel electron energy loss point spectra of this sample indicated that the C phase also contained trace amounts of Pt. Particles of C with diameters of 0.5 to 2.0 nm were also distributed throughout the otherwise unreacted Pt film.

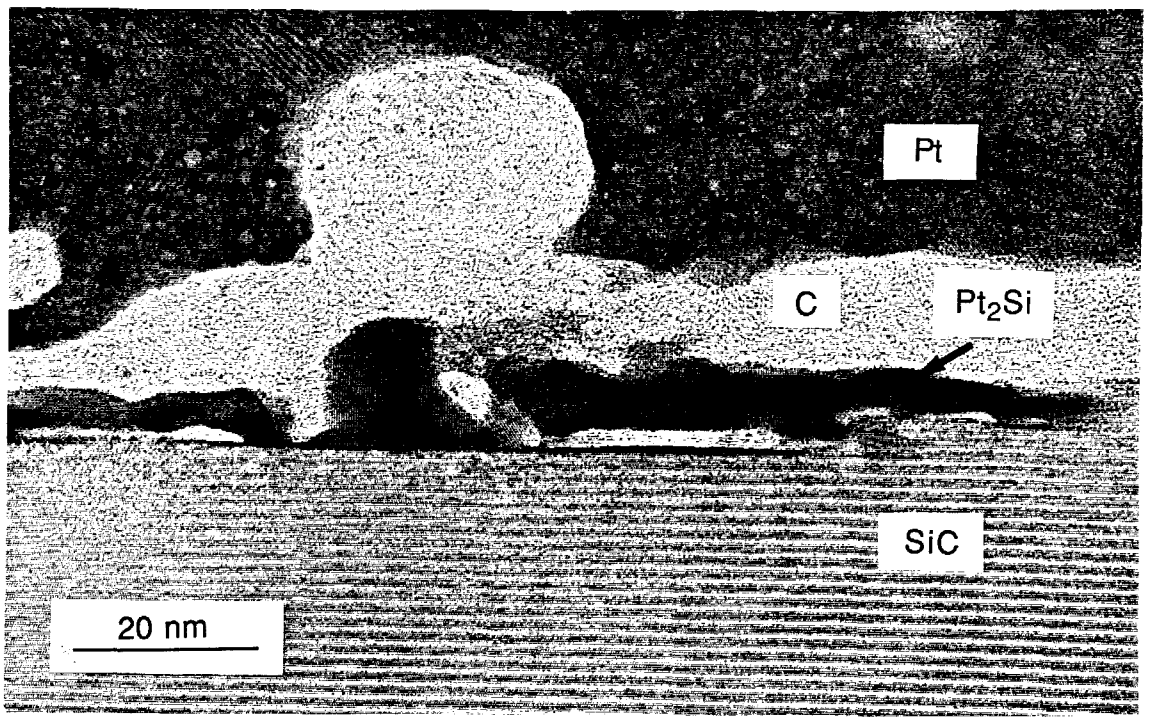

Figure 8. High resolution TEM image of the Pt/SiC interface after annealing at 750°C for 20 min.

Two sets of orthogonal d-spacings of 0.2015 and 0.2785 nm were measured from both optical digital diffraction patterns and micro-diffraction patterns. These experimentally determined d-spacings matched within 0.5% the orthogonal planes with d-spacings $d_{(1\bar{1}2)} = 0.2025$ nm and $d_{(110)} = 0.2781$ nm in Pt_2Si. The platinum silicide was epitaxially related to the SiC with $[1\bar{1}2)_{Pt_2Si} \parallel [0001]_{SiC}$ and $[110]_{Pt_2Si} \parallel [1\bar{1}00]_{SiC}$.

It can also be seen from Fig. 8 that neither the amorphous phase nor the Pt_2Si phase was completely isolated from either the Pt or the SiC. Most of the SiC contacted Pt_2Si. However, there were also some regions where the amorphous C phase made contact with the SiC. There were also tunnels (darker gray) through the C-rich phase where Pt_2Si connected to the Pt phase. The most important interface in terms of electrical properties is, of course, the interface with SiC. As discussed above, most of this interface was comprised of epitaxial Pt_2Si,

indicating that most of the interface has very high structural quality. On the other hand, the C phase which comprises the remainder of the interface has not resulted in a degradation in the electrical properties of the annealed contacts.

These results are to be compared with those of Chou [1] who produced diffusion couples from hot-pressed β-SiC and Pt of about 1 to 2 mm thickness and annealed them in flowing He at 900 and 1000°C for various times. Scanning electron microscopy and energy dispersive spectrometry showed that the interface contained periodic layers of Pt_3Si and C. Pt_2Si did not form until after annealing at 1000°C for an unspecified time. These results are in contrast to the results in the present study in which Pt_2Si, the first silicide observed, formed at 750°C. Differences between these two studies include the SiC polytypes, sample thicknesses, and the annealing conditions. All or one of these differences may explain the differing results; however a definitive explanation based on the research performed is not known at this time.

Localized chemical bonding at the interface for the as-deposited interface was investigated with XPS. Platinum-carbon bonding was not expected to form since there are no equilibrium platinum carbides [14], and the Pt-C bond has been theoretically determined to be very weak.[15] As expected, only C-Si bonding was displayed in the C 1s peak after depositing 4, 8, or 12 Å of Pt. The shifts in the C 1s and Si 2p binding energies (Fig. 5) are attributed to changes in band bending.

The results regarding silicide formation were somewhat inconclusive. Deconvolution of the Pt $4f_{7/2}$ and $4f_{5/2}$ peaks revealed two chemical bonding states. The binding energy due to the major bonding state was 70.94 - 71.58 eV, and that for the minor bonding state was 72.12 - 72.76 eV. The major bonding state is attributed to Pt-Pt bonding.[16] The minor peak at the higher binding energy could be due to either Pt-Si [16] or Pt-O bonding. The reported Si 2p binding energies for Si-bound-to-Pt in Pt silicide (e.g., Pt_2Si and PtSi [16]) and for Si-bound-to-C in SiC [17] are virtually identical. Therefore, it cannot be confirmed from the Si 2p peak whether a Pt silicide formed. There is, however, indication from the Si 2p peak that the oxygen present at the SiC surface before deposition of Pt remained at the interface after the depositions.

Bermudez and Kaplan [3] thermally evaporated thin layers (≤ 8 Å) of Pt onto β-SiC (001). Preliminary results for Pt on β-SiC (111) and α-SiC (0001) were also reported. Prior to deposition of Pt, the substrates were dipped in HF and cleaned in alcohol. An atomic oxygen concentration of 3.5% was found in all Pt films deposited on β-SiC (001) substrates at low temperature (sample temp. $\approx$ 270°C due to radiative heating from the Pt source). Somewhat smaller oxygen concentrations (2.5%) were found in films deposited on α-SiC (0001). The authors suggested that the O contamination resulted from "dissociative adsorption of H_2O in the UHV background."

In the unannealed Pt films deposited in this work, a trace amount of O (≈3 at. %) localized at the interface was detected by PEELS. This result is in good agreement with that of Bermudez and Kaplan and indicates that Pt-O bonding contributed to the second bonding state revealed in the XPS analyses. However, considering the ≈ 30% contribution of the minor Pt $4f_{7/2}$ peak to the total integrated peak area, Pt-Si bonding was also likely present. Furthermore, the fact that the percent contribution did not decrease significantly with increasing Pt thickness suggests that there may have been some intermixing of Pt and Si.

D. Conclusions

A study of the chemistry, microstructure, and electrical properties at interfaces between Pt and monocrystalline, n-type 6H-SiC (0001) was performed for the specific application of contacts in SiC devices. The room temperature deposition of Pt by UHV electron beam evaporation onto these chemically and thermally cleaned substrates resulted in excellent Schottky contacts, which were characterized by low ideality factors ($n < 1.1$) and leakage currents of 5×10^{-8} A/cm^2 at -10 V. The SBH's calculated from I-V measurements (1.06 to 1.26 eV) increased after each successive 20 min. anneal at 450, 550, 650, and 750°C with a corresponding reduction in the leakage currents.

The as-deposited films were polycrystalline with an average grain size of 10 ± 3 nm. Increasing the annealing temperature from 450 to 650°C caused the [111] Pt grains to grow at the expense of the other grains to an average size of 65 nm. The increase in the SBH's calculated from I-V measurements was attributed to this grain growth and corresponding increase in the film homogeneity.

The first reaction phases, crystalline Pt_2Si and an amorphous C phase, were observed to form between the Pt and the SiC after annealing at 750°C. The interfacial reaction should reduce any adherence problems associated with Pt contacts deposited in non-UHV environments, a problem which has been expressed by a number of scientists. In this study the excellent electrical properties after annealing have shown Pt to be a viable choice for Schottky contacts in SiC devices.

E. Future Research Plans and Goals

The current technology of SiC devices is driving the need for ohmic contacts to p-type SiC which have low contact resistivities at both room and elevated temperatures. Aluminum alloys are currently used because the Al degeneratively dopes the surface of the SiC, which reduces the contact resistance. However, these contacts cause problems at elevated temperatures due to melting and extensive diffusion.

We are currently investigating three metal systems, one of which should be much more stable at elevated temperatures. The materials, which are comprised of 2-3 components, were chosen based on chemistry and doping considerations in addition to thermal stability. All three

contact materials have been deposited onto p-type (and in one case n-type) 6H-SiC and have been characterized electrically after annealing at low-moderate temperatures.

Annealing at or near 1000°C has been performed on the contact material with high thermal stability. This system has already shown ohmic behavior. Once the preliminary studies involving annealing conditions and electrical properties have been performed, the chemistry and physics of these interfaces will be thoroughly investigated to understand the mechanisms related to the electrical behavior. The contact resistivity will also be measured as a function of both carrier concentration and temperature.

F. Acknowledgments

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